AD 297 400

NOLTR 62-171

DIFAIR, AN ADJUSTABLE DIGITAL FILTER

27 SEPTEMBER 1962

NOL
UNITED STATES NAVAL ORDNANCE LABORATORY, WHITE OAK, MARYLAND

NOLTR 62-171

NOLTR 62-171

DIFAIR, An Adjustable Digital Filter

Prepared by:

C. N. Pryor

Approved by: T. F. Johnston
T. F. JOHNSTON, Chief
Acoustics Division

ABSTRACT: Many signal processing operations, such as matched filtering, call for filters having specific characteristics. These characteristics may be specified in terms of the impulse response of the filter. The present device simulates such filters by means of high-speed digital computation of the convolution integral once the desired impulse response is set into the selector switches. The circuitry, overall characteristics and several applications of the equipment are described.

PUBLISHED NOVEMBER 1962

U. S. NAVAL ORDNANCE LABORATORY
White Oak, Maryland

NOLTR 62-171 September 27, 1962

This report describes a new approach to the design of generalized filters. The filter is adjusted by changing the settings of impulse response switches and, in the case of a matched filter, it has a frequency response equal to the amplitude spectrum of the waveform to be filtered. The work on DIFAIR was performed under "PUFFS Technical Direction", Task No. RUSD-4C000-150. The report will be of interest to electronic engineers and scientists designing or using matched filters or generalized filters.

R. E. ODENING

Z. I. SLAWSKY
By direction

TABLE OF CONTENTS

ILLUSTRATIONS

DIFAIR, AN ADJUSTABLE DIGITAL FILTER

INTRODUCTION

1. Often a signal filter is desired which can have a very general response characteristic, with a convenient way of adjusting this response. This may be used for studying the effect of various filters on a known signal, or it may be used in signal processing problems as a "matched filter" for detecting a pulse of known characteristics. In the latter problem, particularly, the desired filter characteristic is more easily found in the time domain; and so it becomes desirable to specify the filter in terms of its impulse response rather than its equivalent frequency response.

GENERAL DIFAIR CONCEPT

2. An adjustable filter such as that shown in Figure 1 can be conceived for realizing general impulse responses which vanish (at least approximately) after a finite time. Since the signal at the time t on a given tap n of the delay line is f(t-nT), the output of the system may be written

$$g(t) = \sum_{n=0}^{N-1} h(nT)\, f(t-nT)$$

This is the discrete analogue of the convolution integral giving the output g(t) of a filter with impulse response h(t) and input f(t):

$$g(t) = \int_0^{\infty} h(u)\, f(t-u)\, du$$

Thus the settings of the coefficient potentionmeters h(nT) correspond to the value of the impulse response h(u) at discrete points.

3. Practical considerations and increased range of operation make it desirable to use something other than a passive delay line for delaying the signal to the coefficient pots. A digital shift register is a reasonable choice since the delay per tap, T, is readily variable with shift pulse frequency.

However, the choice of the shift register necessitates converting the input analog signal into a digital code for transmission down the digital delay line, Since the signal into the coefficient pot is now digital rather than analog, it seems reasonable that the coefficient h(nT) should also be specified in a digital form. This choice is also made to allow expansion to a more general system in which the coefficients are determined by performance feedback from the filter output, and thus are computed by the filter. Now the coefficient pots are replaced by digital multipliers; and the outputs of the multipliers may be converted back to analog form and added to produce the filter output. The resultant system is shown in Figure 2.

4. The digital multiplier is the most complex single part of the system, so we wish to reduce the number of multipliers in the system by time-sharing a single multiplier among all the output taps. This may be done by using a system similar to the DELTICS[1] for time compression of the input signal. Consider a system of the form shown in Figure 3. The shift registers contain N-1 stages, and the sample pulses occur every N shift pulses. At the instant a sample pulse occurs (immediately before shifting) the A-D converter contains the present value of the input and the shift registers contain the last N-1 samples of the input in increasing order of age. When the shift pulse occurs, the oldest sample in the shift registers is discarded and the new value of the input is inserted in its place. The sample pulse is then returned to zero, and the next N-1 shift pulses simply rotate the information stored in the shift registers. At the end of N cycles the information in the shift registers is again in the order of increasing age and another new sample can be inserted to replace the oldest one. During this interval, every one of the last N samples has been shifted past the output of the DELTIC loop in order from the oldest to the newest (that is, in decreasing order of n). The DELTIC has simultaneously up-dated its information so that the samples appearing at the output will always be the most recent N samples. It is evident that the shift pulses must occur at N times the rate of the sample pulses and that the interval between sample pulses in T.

5. During the interval between sample pulses an N-word digital memory representing the impulse response may be read from the impulse response generator. If this is read in decreasing order of n and fed to the multiplier along with the

1. NAVORD Report 4244, "Delay Line Time Compressor XT-1A", J. C. Munson and L. E. Barton, 6 Sept. 1956.

output of the DELTIC loops, the instantaneous product h(nT) f(t-nT) will be formed. Summing the outputs of the multiplier over the interval between sample periods gives the desired output

$$g(t) = \sum_{b=0}^{N-1} h(nT)\, f(t-nT)$$

The summing operation may be accomplished by converting back to analog form and averaging with a time constant of approximately T.

DIFAIR CHARACTERISTICS

6. The DIFAIR block diagram, using the techniques described above, is shown in Figure 4. The number of delay points N in the impulse response is set at 32, and all digital quantities are characterized by 4-bit binary numbers. The entire system, except for one special card, is constructed from Computer Control Corporation "S-Pacs"[2] and is shown in Figure 5. Detailed diagrams are shown in Figures 6 through 9. Operating controls consist of an input gain control, coarse and fine clock frequency controls, and a bank of thirty-two 15-position switches for setting in the impulse response. Input to the system should be at least 1 volt rms, and the DC gain of the system may be figured approximately as

$$\text{Gain (dc)} = \frac{\text{Sum of impulse response switch settings}}{54}$$

The frequency range of the filter is determined by the sample pulse frequency, which can be varied from 1.25 cps to 23 kilocycles according to the frequency selector switch setting as shown in Table 1. Actual frequencies may vary somewhat from those shown, since the clock is a multivibrator. Continuously variable frequencies are available by means of a potentiometer on the multivibrator card. The amplitude of each of 32 equally spaced points is set to any of 15 values between plus and minus 7 units by means of the switches on the impulse response selector panel. The upper left switch controls h(32T), and the delay taps are arranged in decreasing order across the four rows,

2. Pub. No. 71-100A, "Instruction Manual for S-PAC Digital Modules", Computer Control Co., Inc., Framingham, Mass., 11 Apr. 1962.

reaching h(T) in the lower right corner.

7. Since DIFAIR operates on sampled data, some means of reconstructing the sampled output into a continuous form is necessary. It is also necessary to insure that the frequency range of the input data is limited to something less than one-half the sampling frequency. It is intended that both these operations be handled by sharp cutoff low pass filters on the input and output of the DIFAIR equipment. These filters are not included in DIFAIR itself because of the wide range of sampling frequencies available, and must be provided by the user. Filters such as the SKL Model 302, set at approximately 40% of the sampling frequency, should be satisfactory for most applications.

8. As in any digital system, a certain amount of noise is introduced by the finite number of quantizing lecels used. The output of the D-A converter is quantized into 1.4 volt steps, which gives an rms output quantizing noise of $1.4/\sqrt{12}$ or 0.4 volts (assuming rectangular distribution of the quantizing noise). If the clock frequency is C and the quantizing noise is assumed independent between samples the low-frequency noise power spectrum out of the D-A converter is $(0.4)2/C$ volts^2/cps. If the output filter is set to cut off everything above half the sampling frequency (Nyquist rate), the noise out of the filter will be $(0.4)^2/C$ S/2. But the sampling rate S is C/32, and the total noise out is thus $(0.4)^2/64$ volts^2 or 0.05 volts rms. Typically the signal output will be on the order of 1 volt, so that the signal-to-quantizing noise ratio at the output will be on the order of 26 db.

COMPONENTS OF DIFAIR SYSTEM

9. The multiplier is the most complex single part of the DIFAIR system. It must produce a digital output equal to the product of the 4-bit digital inputs from the DELTIC loops and from the impulse response generator. Since a 4-bit output resolution was considered sufficient from the multiplier, the problem becomes one of specifying four functions of eight input variables. However, if the inputs and the output are in the form of a sign bit and three magnitude bits, the magnitude output of the multiplier can be specified by three functions of six variables. Since this is a marked simplification of the problem, the sign-magnitude method was chosen for coding the multiplier input and output. The largest possible input or output of the multiplier is a "7", so the scaling of the multiplier was set such that

Output = (Input 1) (Input 2)/7.

Fractional parts of the scaled product were rounded to the nearest integer, and the multiplier characteristics were thus defined as in Table 2. From this table, the logical functions defining the output were found and minimized and are shown in Table 2. Assuming all complements of the inputs to be available the high bit X of the output required 12 gates and diode clusters for realization, the Y bit required 19, and the Z bit required 33; for a total of 8 cards of S-Pac logic in the multiplier.

10. The output digital-to-analog converter uses a resistor summing network to produce a voltage proportional to the digital output of the multiplier. Since D-A conversion is performed more easily if the negative numbers are stored in complementary fashion, it was decided that such a number system should be used here. Conversion of sign-magnitude codes into the "1's complement" form is accomplished simply by complementing all the magnitude bits of the number if the sign is negative and the multiplier output is thus converted to 1's complement form before being sent to the D-A converter. The D-A conversion itself is accomplished by resistors having conductance ratios of 7:4:2:1 connected to the sign and progressively less significant magnitude bits of the 1's complement number. A constant 7 is subtracted from this result to center the output around zero volts and give a range from plus 7 to minus 7. Note there are two ways in which a "zero" output can occur; a "plus zero" (1000), or a "minus zero" (0111). This is inherent in the sign-magnitude, and thus in the 1's complement, code.

11. The analog-to-digital converter which converts the input signal to digital form also uses the 1's complement code for its binary output. The converter uses a feedback principle in that it generates a proposed digital output, converts it back to analog form through a resistor summing matrix, and feeds back the analog output for comparison with the analog input signal. The results of this comparison determine the next digital output to be tried by the converter.

12. The first output tried during a conversion operation is a 1000 or a plus zero. This is converted back to an analog zero and compared with the input voltage. If the input is greater (more negative) than the fed-back voltage, it is evident that the "7" bit of the output must be left on. Otherwise it is turned off. On the next cycle of the conversion the "4" bit is turned on so that the state of the converter output is either 1100 or 0100, depending on the outcome of the first comparison. Again the fed-back voltage is compared with the

input signal to determine whether the "4" bit should be left on. The same procedure is then tried with the "2" bit, and finally with the "1" bit. The converter thus progressively divides up the range of allowed input voltages by assuming a value in the center of the range of uncertainty and determining whether the actual input is above or below this value. The analog feedback is biased such that input voltages between plus and minus one-half unit (one unit is about 0.23 volts) are coded as plus zeros (1000), voltages between plus one-half and plus one and one-half units are coded as plus one (1001), etc. Any voltage in excess of plus 6 1/2 units (approx. 1.5 volts) is coded as a plus "7" (1111), while those below minus 6 1/2 units are coded as minus "7" (0000). An overflow indicator is provided which lights whenever a plus or minus "7" occurs at the DELTIC output. The input gain control should be adjusted such that this light flashes occasionally, but does not glow steadily. The converter should not generate a minus zero (0111) when properly adjusted. Examples of the converter operation are shown in Figure 10.

13. Since four decisions are required for a complete conversion and these are done at the clock rate, the sampling aperture is 4/32 or one-eighth of the sampling period. The converter will not necessarily produce the correct output if the input signal changes significantly during the sampling aperture, and introduces a form of harmonic distrotion to the input signal. This is similar, but not identical, to the difficulties introduced in A-D converters employing sample-and-hold circuits when the sampling aperture is a significant part of the sampling period.

14. The DELTIC loops in DIFAIR use shift register stages as the storage and delay elements so that the effective delay down the shift register line may be varied over a wide range according to the clock frequency. There are four separate loops, operating on the four bits of the A-D converter output in parallel fashion. Since there are 32 points selected on the impulse response, the shift registers in the DELTIC loops must each contain N-1 or 31 stages, as discussed in paragraph 4. The DELTIC loops require a total of 36 S-Pacs, including sampling logic and shift register driving amplifiers, or one-half the total number of Pacs in the system. If the DIFAIR system were to operate at a fixed frequency, the DELTICS could be built from fixed acoustic or magnetostrictive delay lines at considerable savings in space. The DELTIC outputs represent a time compressed replica of the last 32 samples of the input signal, beginning with the oldest one at the time of the sample pulse and ending with the most recent sample during the clock period before the next sample pulse. The DELTIC outputs are still in 1's complement form since their inputs come directly from the A-D converter. Thus the outputs are passed through conversion logic to form the required sign-magnitude code

before being passed on to the multiplier.

15. As described in paragraph 5, the impulse response generator must produce a time-compressed image of the impulse response and transmit this image to the multiplier in reversed order, h(32T) being generated at the time of the sample pulse and h(T) immediately before the next sample pulse. The values of the impulse response at each of the 32 points are stored in the bank of impulse response selector switches. Each switch has a single input line and four output lines which represent the four-bit binary number (sign-magnitude coding) set into the switch. If the switch is set at plus 5 (1101), for example, the "+", "4", and "1" output lines are connected to the input line. The switches are sequentially interrogated by a 32 stage shift register running at the clock frequency and connected as a ring counter, only one of whose outputs is at ground at a time. Thus the selected output lines of a given switch will be at ground at the time the switch is interrograted, while all other lines will be open or at minus 6 volts. If all the "1" lines from the 32 switches are fed to a "nand" gate, the "2" lines to another gate, etc., the outputs of the four gates will sequentially represent the settings of the 32 switches; with the output pulse pattern repeating every sampling period. Since the sample pulse is to occur at the same time that h(32T) appears at the output of the impulse response generator, it is obtained from the output of the ring counter that interrogates the h(32T) switch. The remaining switches are then interrogated in order of decreasing delay. Although circuitry is included to insure that no more than a single "1" circulates in the ring counter, it is possible that the ring counter could be forced into a state in which every shift register contained a logical zero, and would remain in this state. The "Restart" button on the main control panel may be used to insert a "1" in the ring counter to restore normal operation in this event.

APPLICATIONS OF DIFAIR

16. The primary application of DIFAIR is in the detection of pulse signals in a noise background through matched filter techniques. It can be shown that the peak output due to the signal pulse divided by the rms noise output (signal-to-noise ratio) due to a white noise background can be maximized by passing the signal and noise through a linear filter whose impulse response h(t) is given by

$$h(t) = s(T_1 - t)$$

where s(t) is the shape of the signal pulse and T_1 is a delay

required to allow physical realizability of the filter. (This operation is exactly equivalent to a continuous crosscorrelation of the input signal and noise with a stored replica of the signal waveform.) Since for these problems the required filter characteristics are specified in terms of the impulse response, the DIFAIR equipment is ideally suited for use. Best performance can be obtained from DIFAIR by adjusting it as follows:

1) Select the portion of the desired pulse waveform that contains the majority of the energy. (Long tails of pulses which contain only a few percent of the total pulse energy can be eliminated without seriously degrading the theoretical performance of the matched filter. With the DIFAIR equipment, using shortest possible sigment of the pulse gives the highest sampling frequency.)

2) Locate the entry in Table 1 which gives a duration of impulse response nearest the length of the pulse segment selected above. This establishes the sampling frequency for the system. The input and output filters should be set to one-half this sampling frequency.

3) Divide the segment of the pulse (having the duration given in Table 1) into 32 equal segments and list the amplitudes of the pulse at these 32 points.

4) Scale these amplitudes so that the largest amplitude is equal to 7 units, and round off each number to the nearest integer. This new list is the list of settings of the impulse response selector switches.

5) Since the impulse response is the "mirror image" of the pulse waveform, the values obtained above should be set into the switches starting in the upper left corner and proceeding across the rows to the lower right.

17. An example of matched filtering is shown in Figure 11. The pulse waveform is a half sine wave, and Figure 11a shows the pulse and corresponding output of the filter with no noise present. This indicates the amount of sampling and quantizing noise present in the output. Note the output is not an exact reproduction of the pulse, but rather is of the form of the autocorrelation function of the input pulse. Figures 11b and 11c then show the input pulse in the presence of noise and the corresponding output of the filter. The test setup for this example is shown in Figure 12.

18. A secondary application of DIFAIR allows a direct measurement of the frequency spectrum of a pulse signal. When DIFAIR is adjusted according to the method specified for matched filtering,

its frequency response is equal to the amplitude spectrum of the selected waveform. The spectrum can therefore be determined simply by measuring the DIFAIR frequency response with an oscillator and AC voltmeter. Of course frequencies above one-half the sampling rate of the system cannot be considered, and some error is to be expected due to quantizing noise and harmonic distortion in the sampler. The spectrum of the half-sine pulse was determined in this manner and plotted in Figure 13, in comparison with the true spectrum obtained by fourier transforming the pulse.

19. An additional application of DIFAIR is in the study of the effect of various filter functions on signals, where the filters may be specified in the time domain. Typical of this is the attempt to produce a low-pass filter with sharp cutoff, while not affecting the symmetry of a transient pulse passed through the filter. Figure 14 shows the frequency response of such a filter, whose impulse response was selected as a truncated $(\sin x)/x$ function. Notice the cutoff is very sharp, but that fairly large lobes exist above the cutoff frequency. These are due largely to the quantizing of the input sinusoid and are strongly dependent on signal amplitude. Thus measurement of the frequency response using white noise input and a spectrum analyzer should yield more valid information about the response, and can be expected to give a smoother response curve above the cutoff frequency than that shown.

POTENTIAL APPLICATIONS

20. While the present form of DIFAIR provides a very flexible piece of laboratory apparatus for simulating desired filter functions and for matched filtering experiments, its capabilities can be extended considerably by allowing the impulse response to be computed from the output of the filter itself. For instance, this allows the filter to form and refine its estimate of the desired signal in certain types of matched filtering operations, so that good estimates of the signal made during times of large signal to noise ratio can help to optimize the system and improve performance during low signal-to-noise ratio periods. It is also felt that an adaptive form of DIFAIR can be built which would automatically compensate for non-white background noise in matched filtering problems, and maintain an optimum system in spite of variations in the background noise spectrum. Other applications or extensions of the DIFAIR system should present themselves through use of the system.

REFERENCES

1. NAVORD Report 4244, "Delay Line Time Compressor XT-1A", J. C. Munson and L. E. Barton, 6 Sept. 1956.

2. Publication No. 71-100A, "Instruction Manual for S-PAC Digital Modules", Computer Control Co., Inc., Framingham, Mass., 11 Apr. 1962.

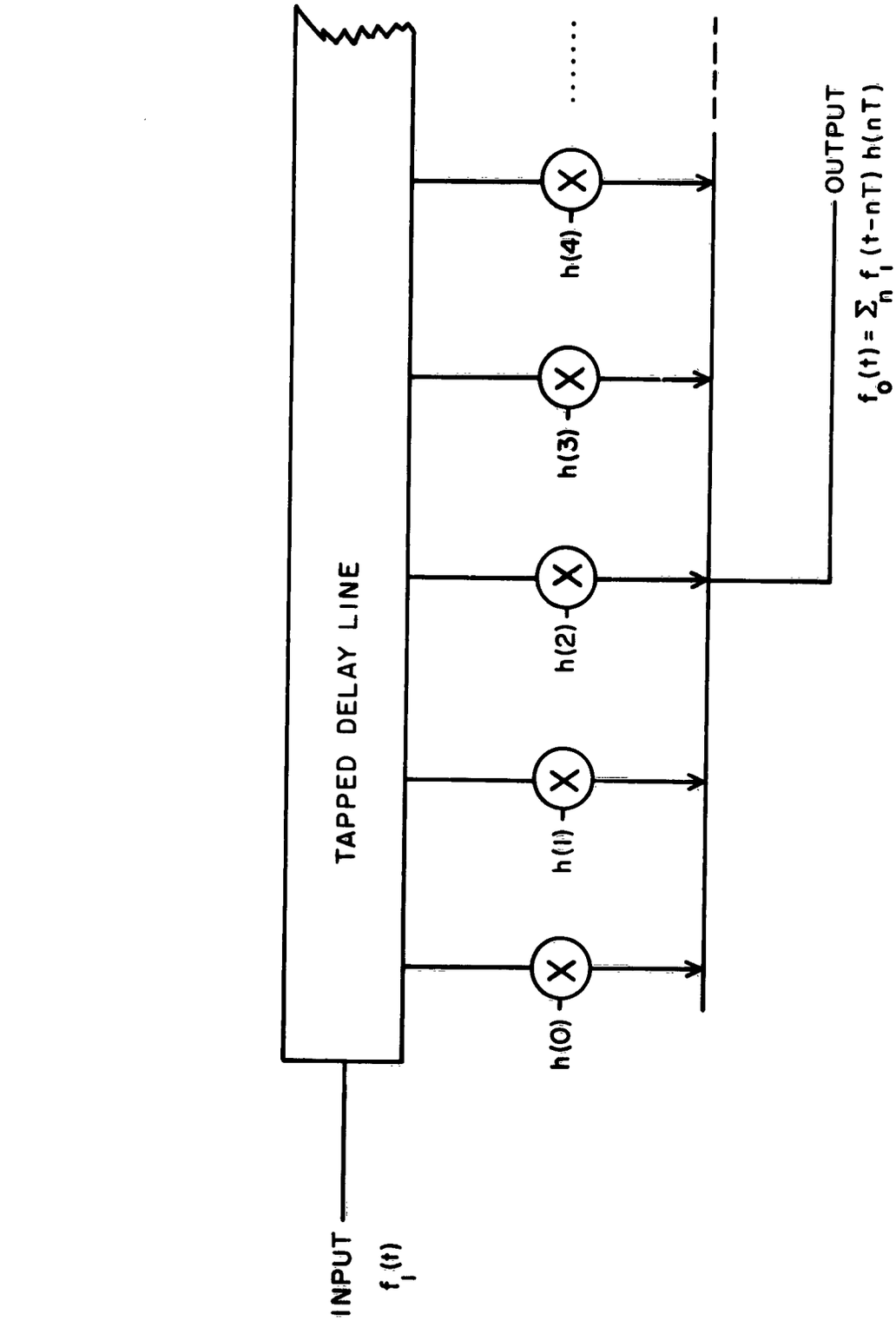


FIG.1 DELAY LINE REALIZATION OF CONVOLUTION EQUATION

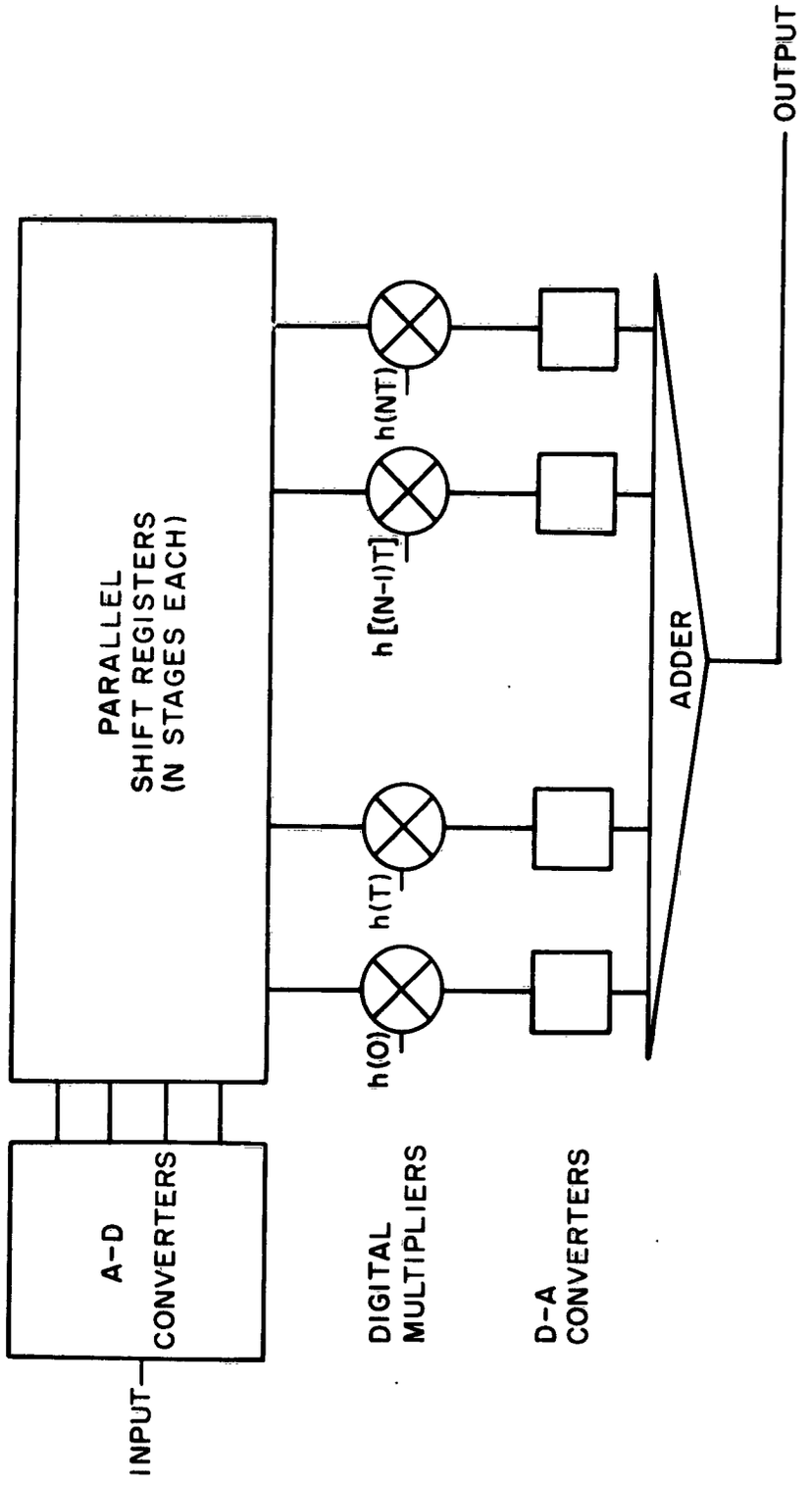


FIG. 2 SYSTEM USING SHIFT REGISTER DELAYS

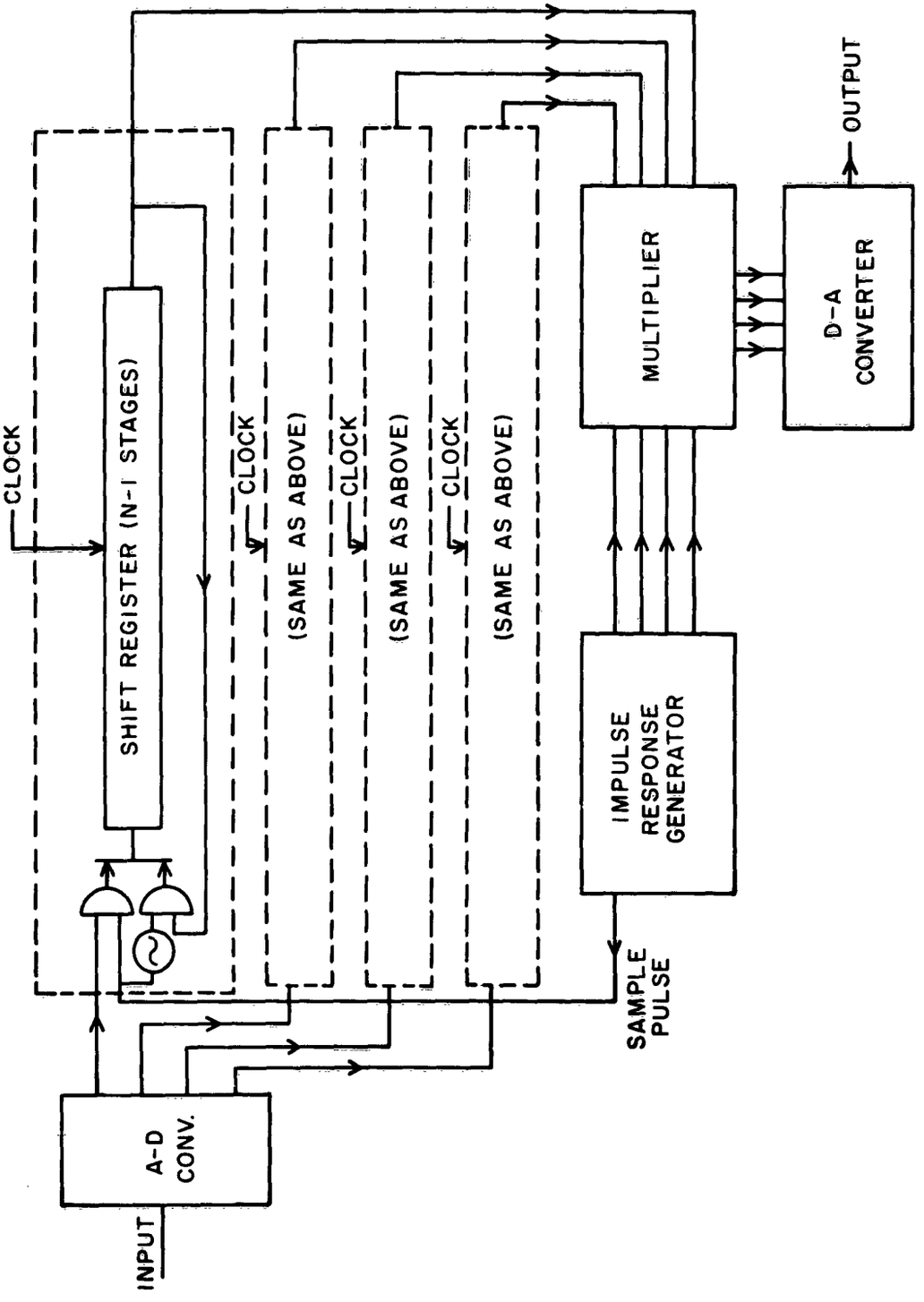


FIG.3 SYSTEM USING TIME COMPRESSION

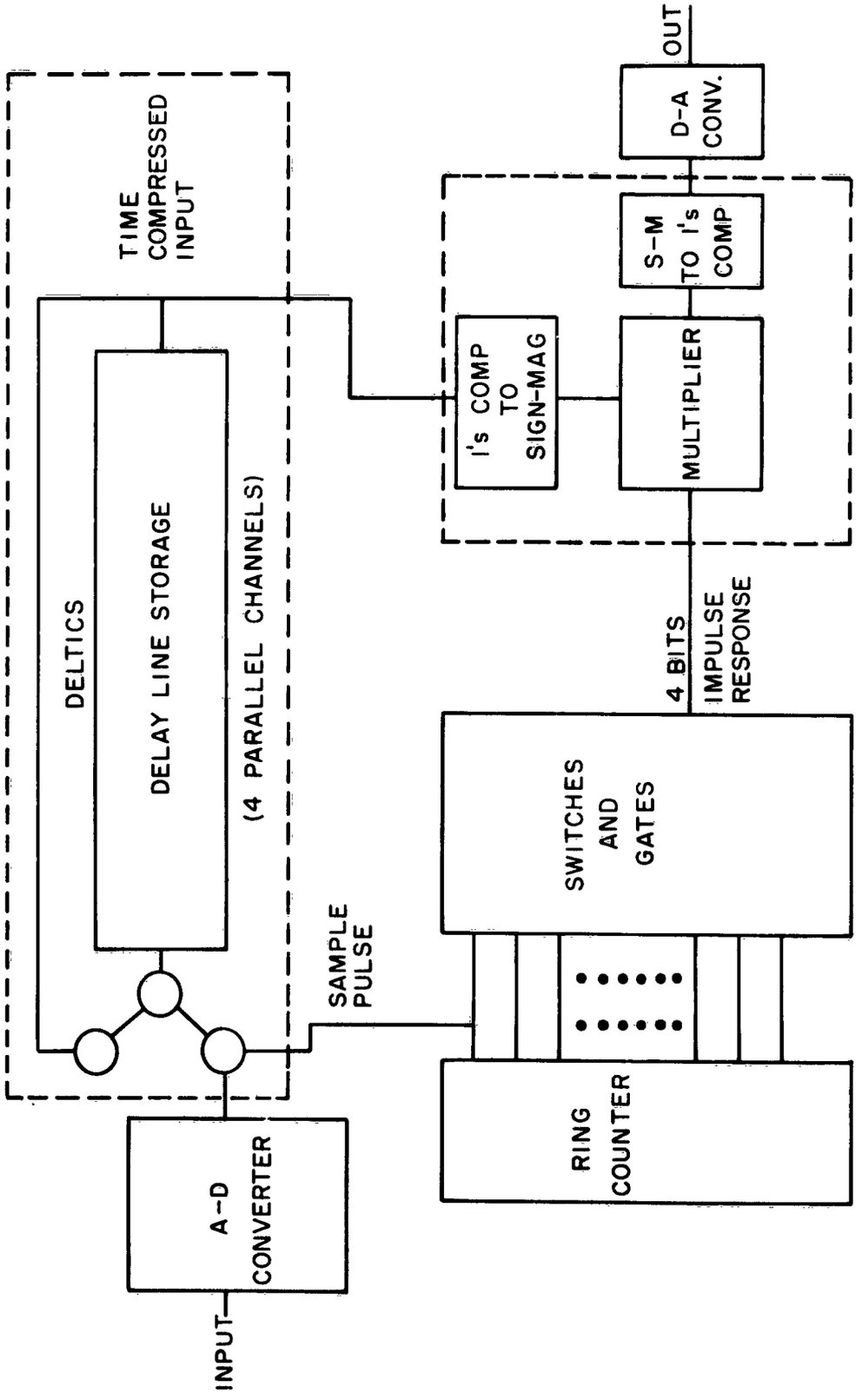


FIG. 4 BASIC DIFAR BLOCK DIAGRAM

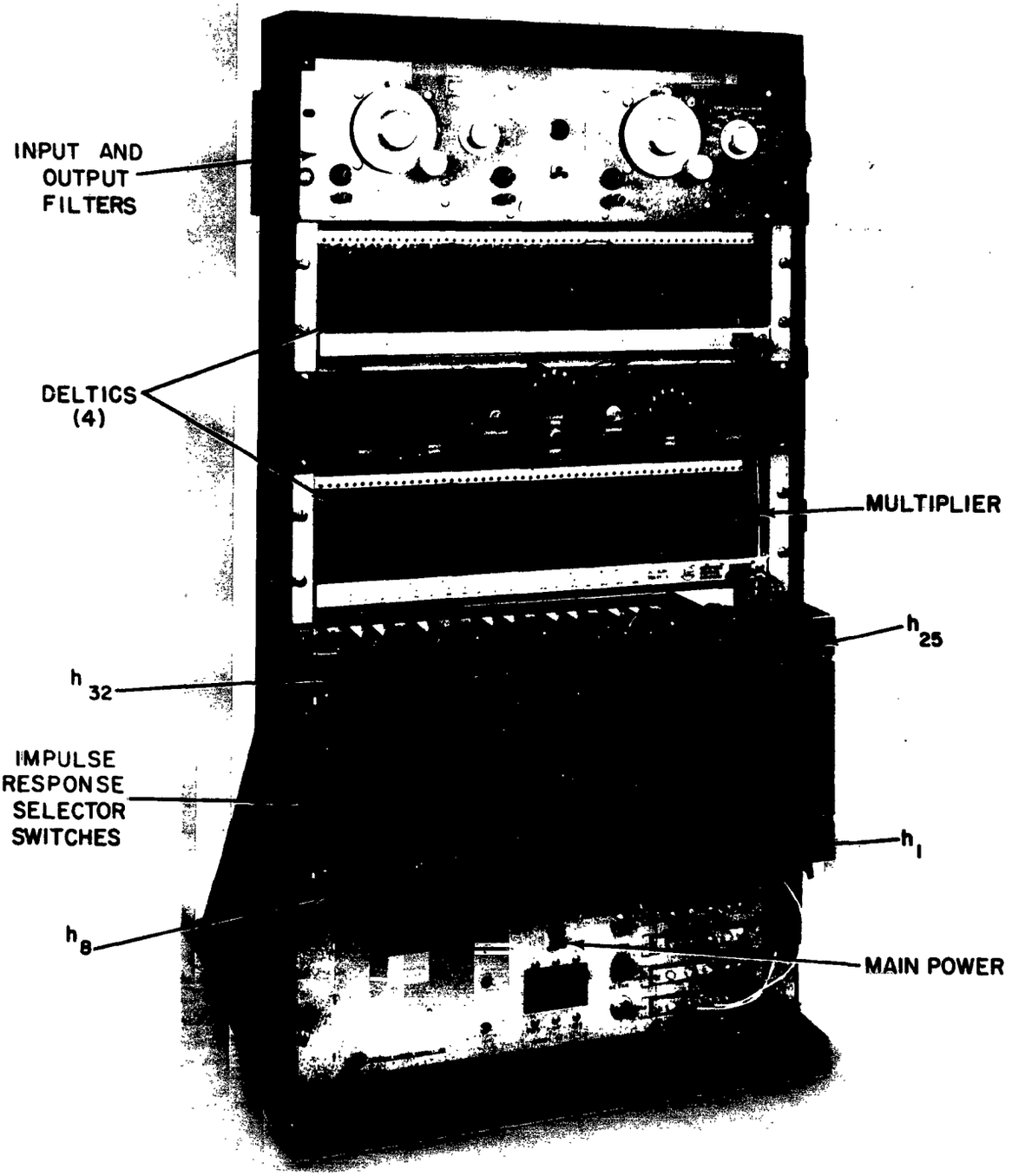
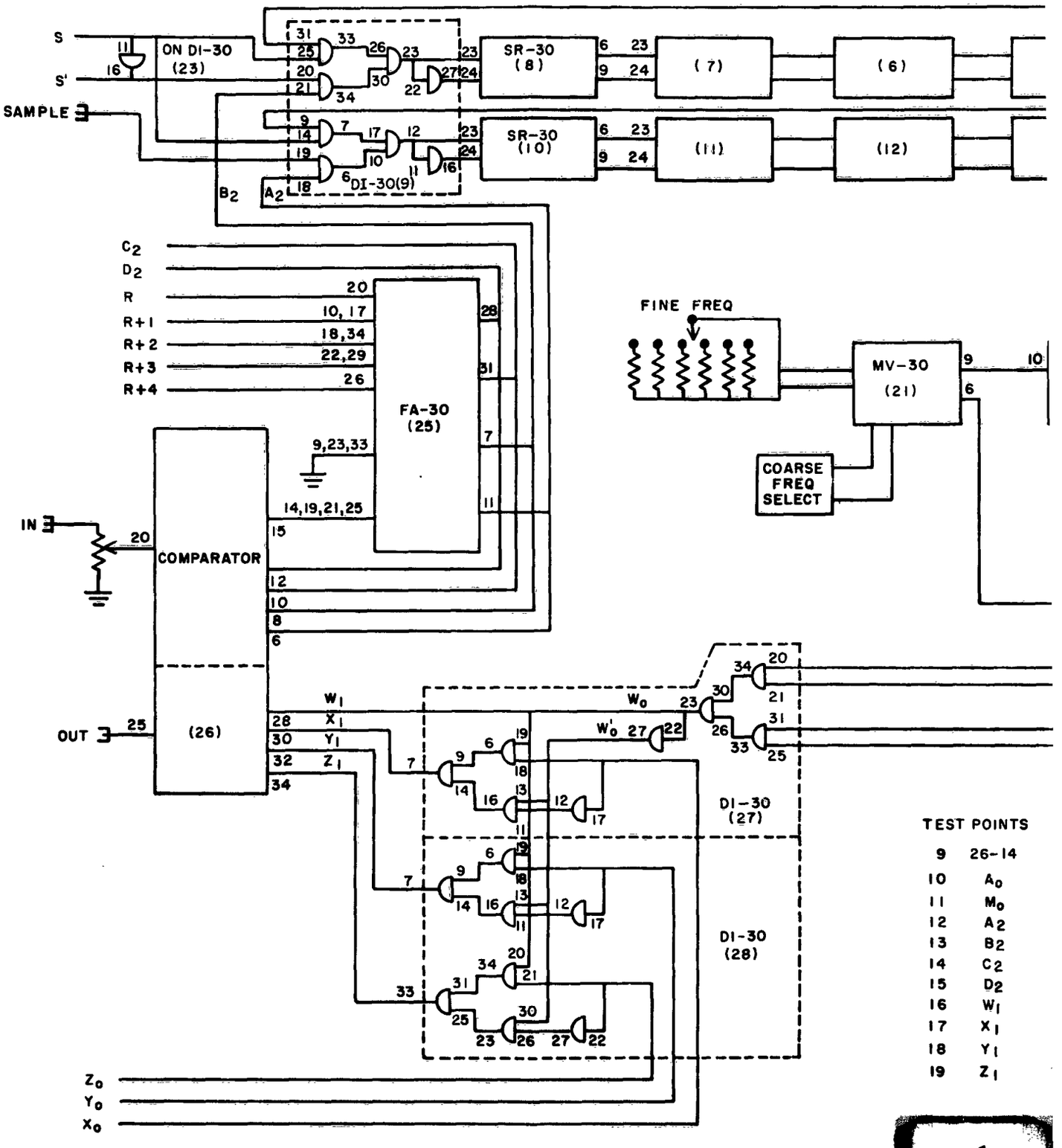
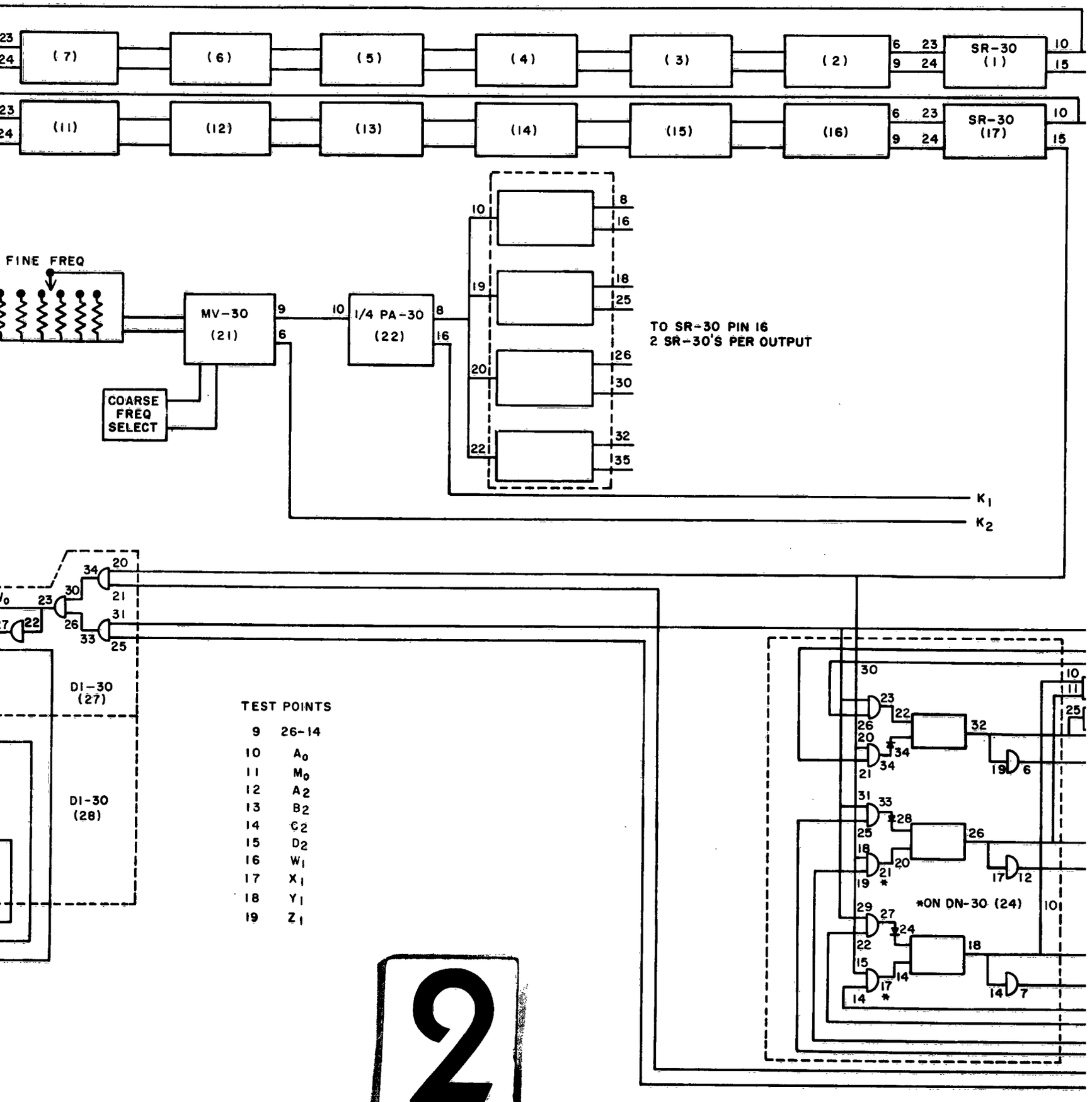


FIG. 5 THE DIFAIR SYSTEM

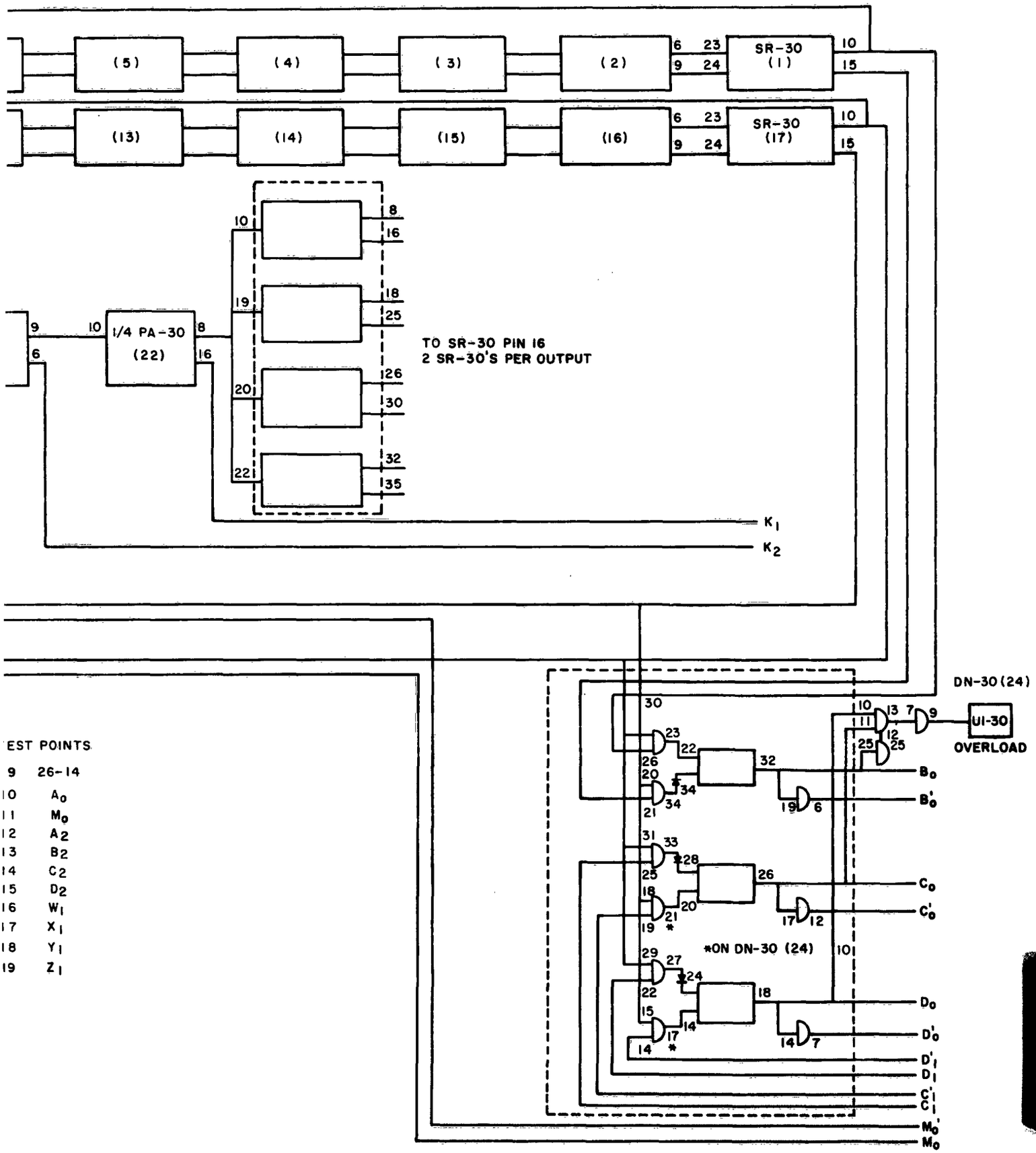


TEST POINTS	
9	26-14
10	A_0
11	M_0
12	A_2
13	B_2
14	C_2
15	D_2
16	W_1
17	X_1
18	Y_1
19	Z_1

FIG. 6 DIFAIR BLOCK I


(7)
(6)
(5)
(4)
(3)
(2)
SR-30 (1)
(11)
(12)
(13)
(14)
(15)
(16)
SR-30 (17)
FINE FREQ
MV-30 (21)
1/4 PA-30 (22)
COARSE FREQ SELECT
TO SR-30 PIN 16
2 SR-30'S PER OUTPUT
K_1
K_2
DI-30 (27)
DI-30 (28)
TEST POINTS
9 26-14
10 A_0
11 M_0
12 A_2
13 B_2
14 C_2
15 D_2
16 W_1
17 X_1
18 Y_1
19 Z_1
*ON DN-30 (24)

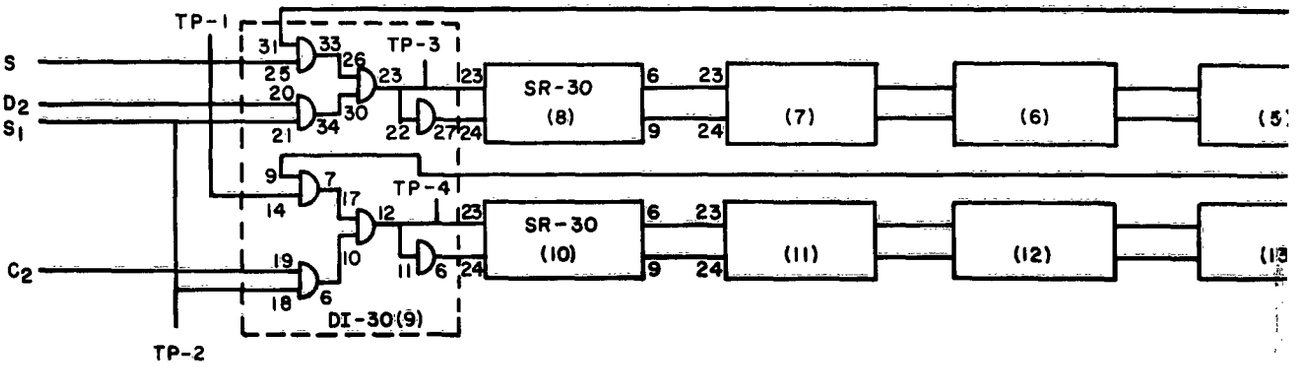
2

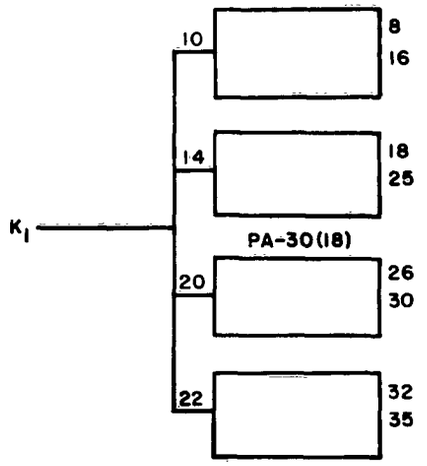


TEST POINTS

9	26-14
10	A_0
11	M_0
12	A_2
13	B_2
14	C_2
15	D_2
16	W_1
17	X_1
18	Y_1
19	Z_1

3





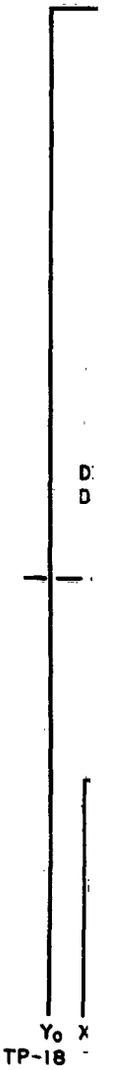
TO SR-30 PIN 1b
2 SR-30 PER OUTPUT

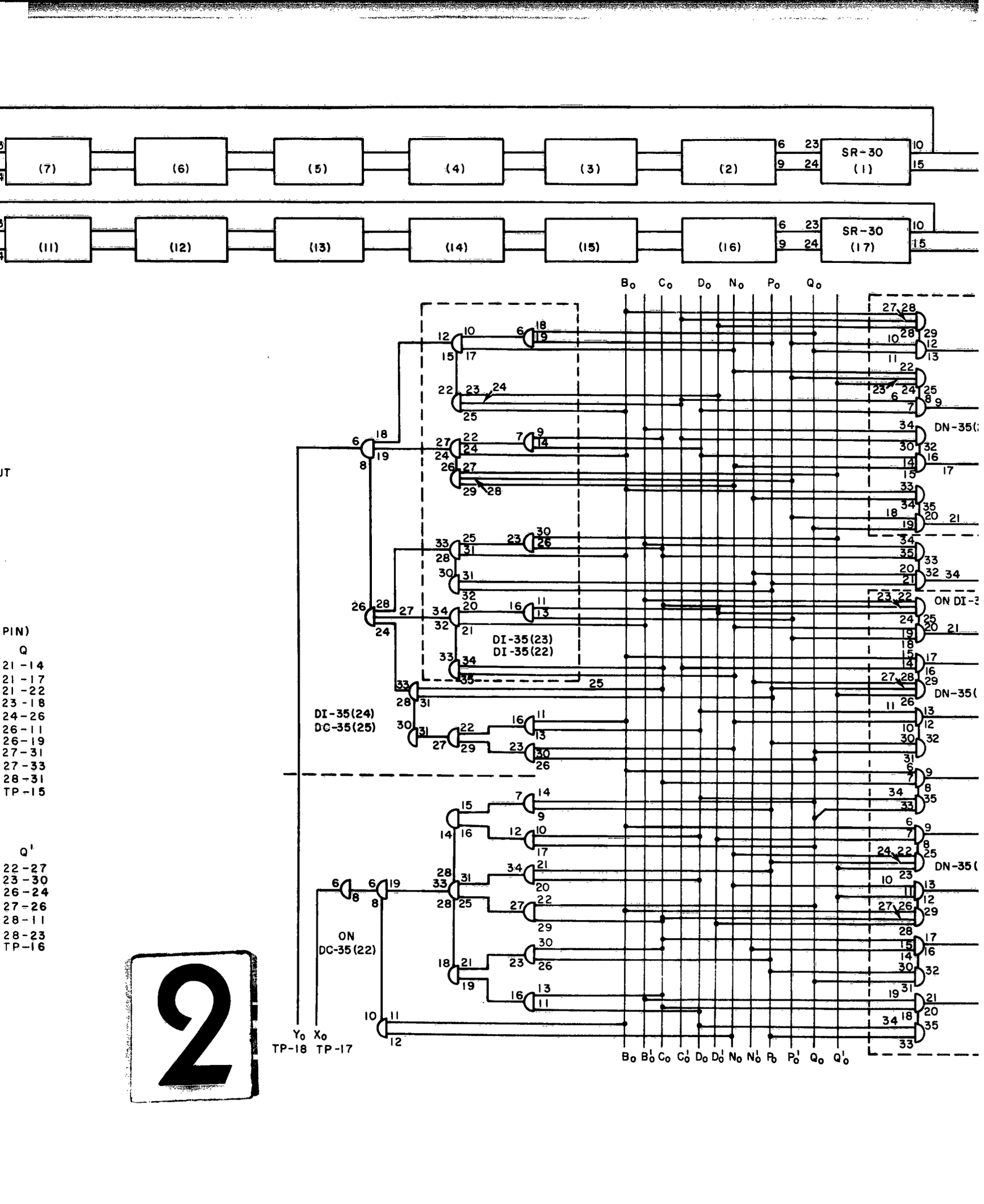
MULTIPLIER INPUT CONNECTIONS (CARD-PIN)

B	C	D	N	P	Q
22-11	21-13	21-10	22-12	21-9	21-14
22-25	21-29	21-11	22-29	21-21	21-17
23-29	21-30	21-20	22-35	21-26	21-22
23-31	22-34	23-14	23-17	22-32	23-18
24-11	23-9	24-13	24-30	23-19	24-26
26-28	24-25	26-7	26-15	24-21	26-11
26-33	25-35	26-14	26-22	24-31	26-19
27-6	27-7	27-11	27-10	27-27	27-31
27-15	27-23	27-34	27-19	27-30	27-33
28-6	28-15	28-34	28-10	28-24	28-31
28-26	28-18	TP-9	28-22	28-30	TP-15
TP-5	28-27		TP-11	28-33	
	TP-7			TP-13	

B'	C'	D'	N'	P'	Q'
23-21	22-24	22-23	22-31	22-28	22-27
25-34	23-26	23-11	24-20	23-13	23-30
26-31	26-6	26-26	26-34	26-10	26-24
27-22	26-27	27-24	27-28	26-18	27-26
28-19	26-30	28-7	28-14	26-23	28-11
TP-6	27-14	28-28	TP-12	27-18	28-23
	TP-8	TP-10		TP-14	TP-16

FIG.7 DIFAIR BLOCK 2



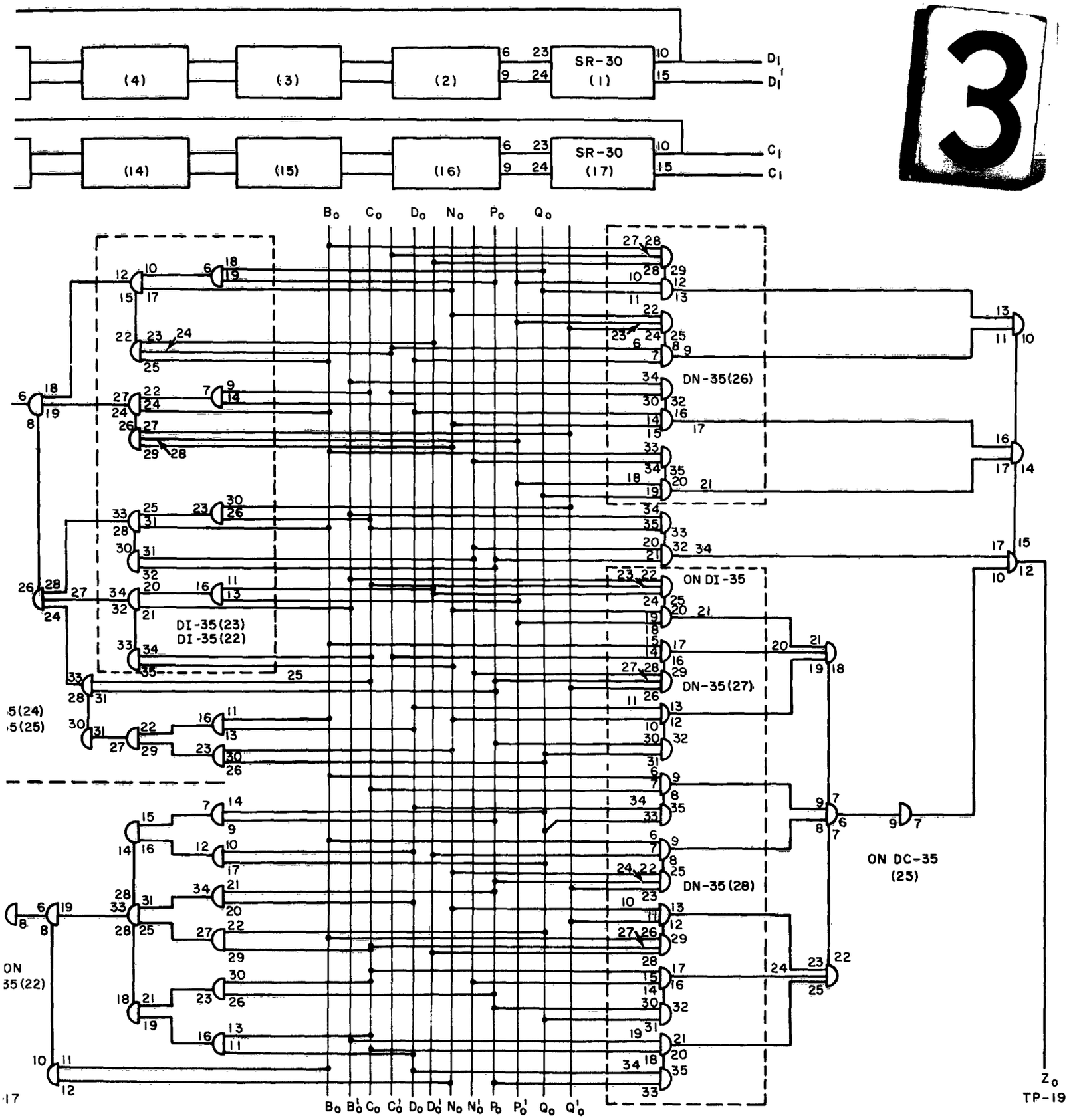


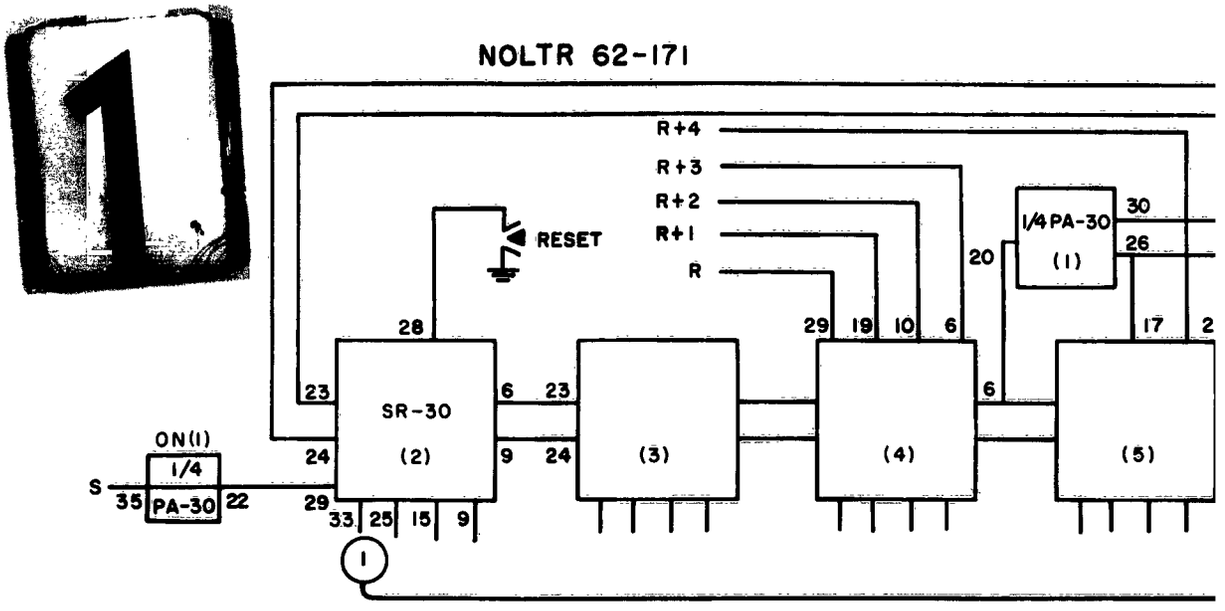
PIN)

Q
21 - 14
21 - 17
21 - 22
23 - 18
24 - 26
26 - 11
26 - 19
27 - 31
27 - 33
28 - 31
TP - 15

Q'
22 - 27
23 - 30
26 - 24
27 - 26
28 - 11
28 - 23
TP - 16

2


(4)
(3)
(2)
SR-30
(1)
D1
D1'
(14)
(15)
(16)
SR-30
(17)
C1
C1'
3
Bo Co Do No Po Qo
DN-35(26)
ON DI-35
DN-35(27)
DN-35(28)
ON DC-35
(25)
DI-35(23)
DI-35(22)
Zo
TP-19
Bo Bo' Co Co' Do Do' No No' Po Po' Qo Qo'



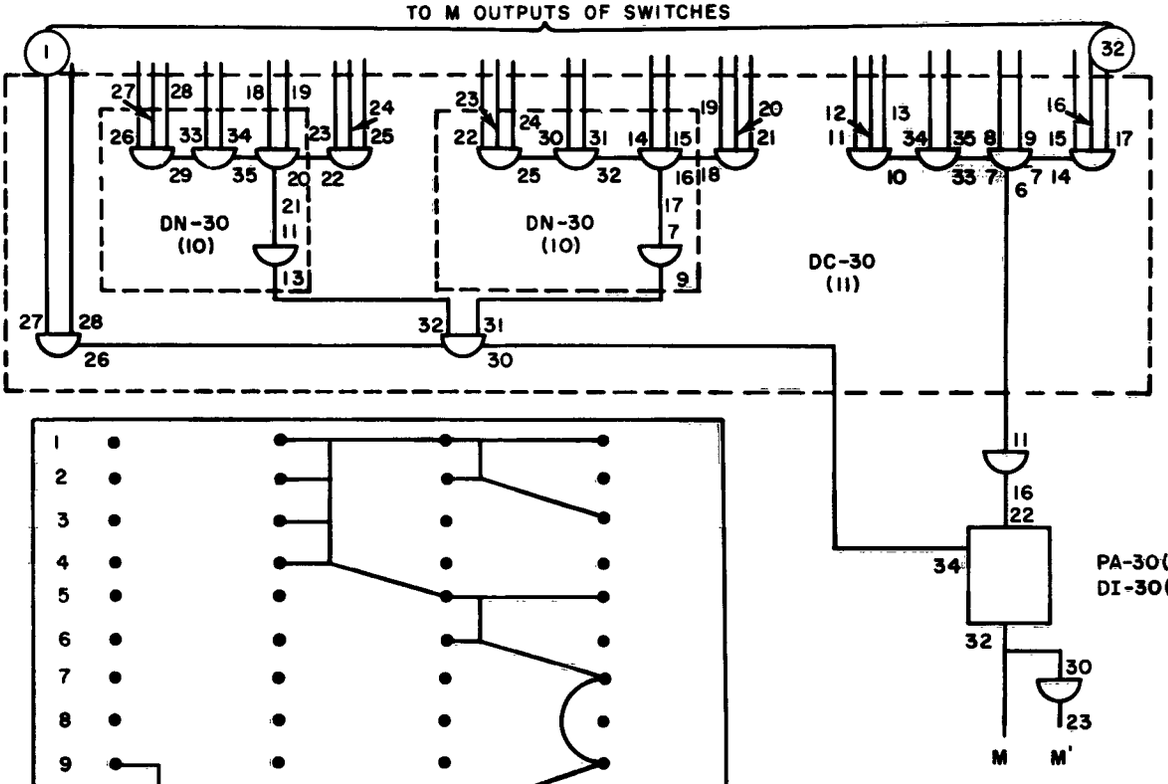


FIG.8 DIFAIR BLOCK

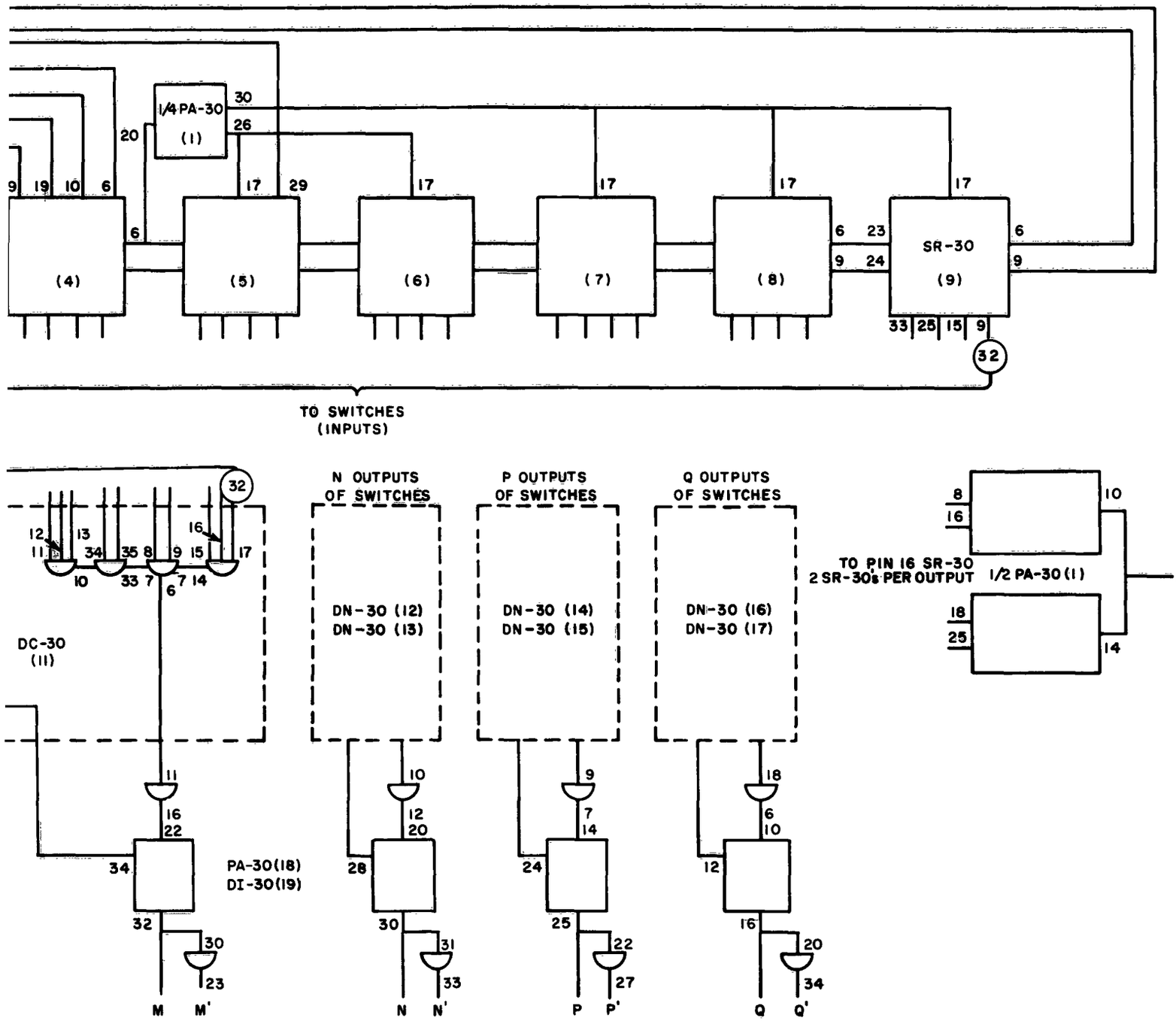


FIG.8 DIFAIR BLOCK 3

2

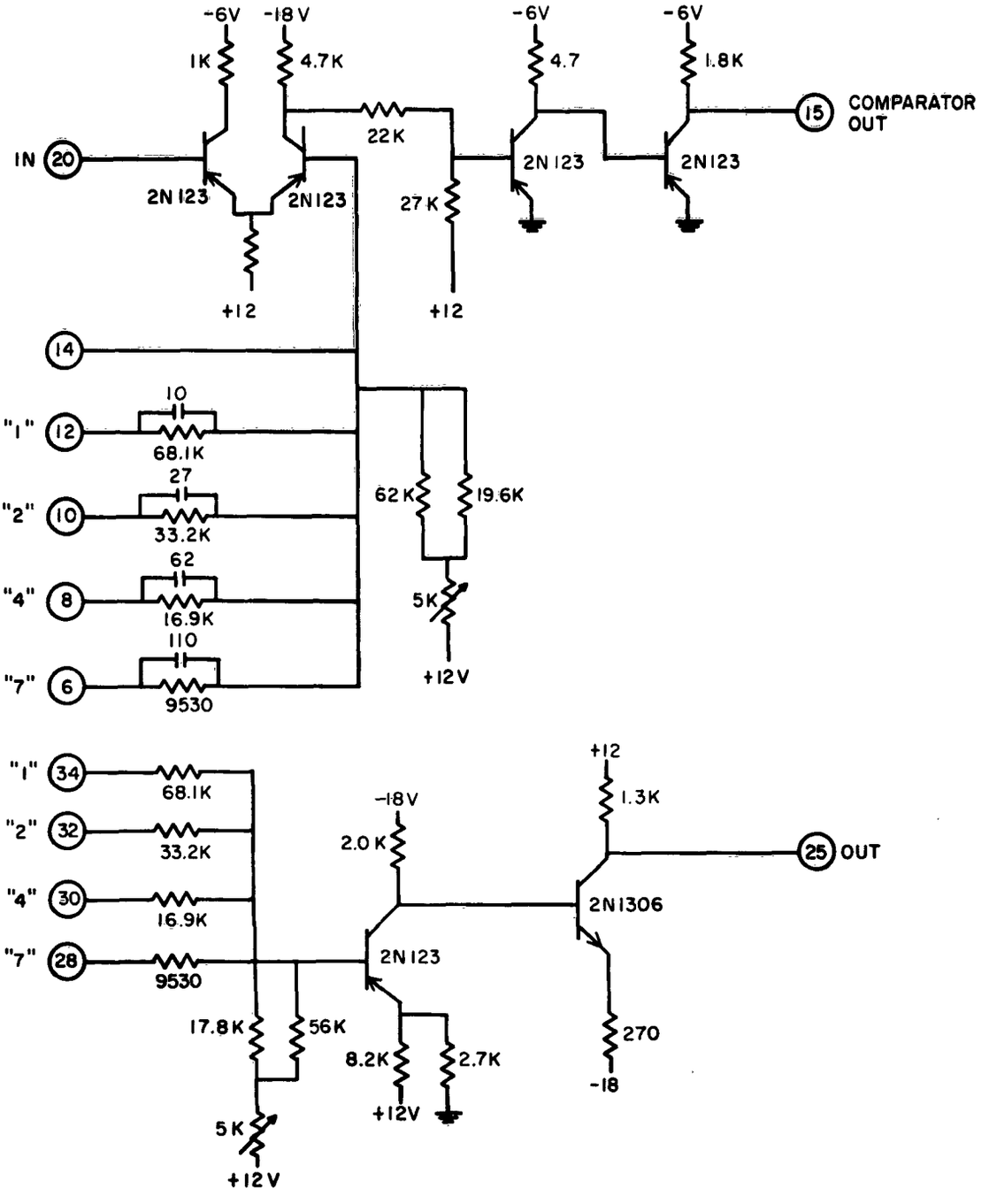
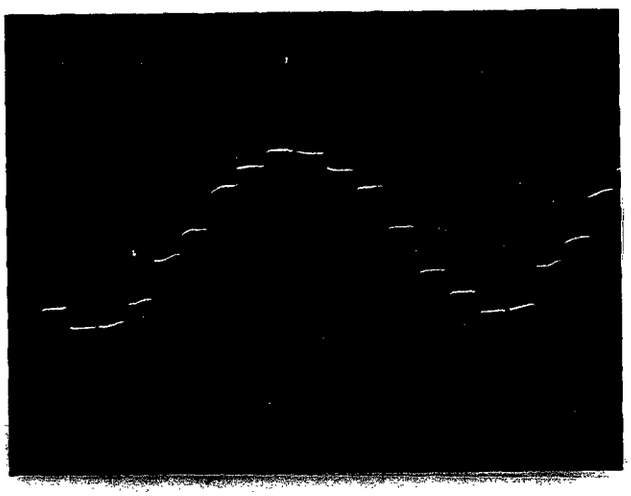
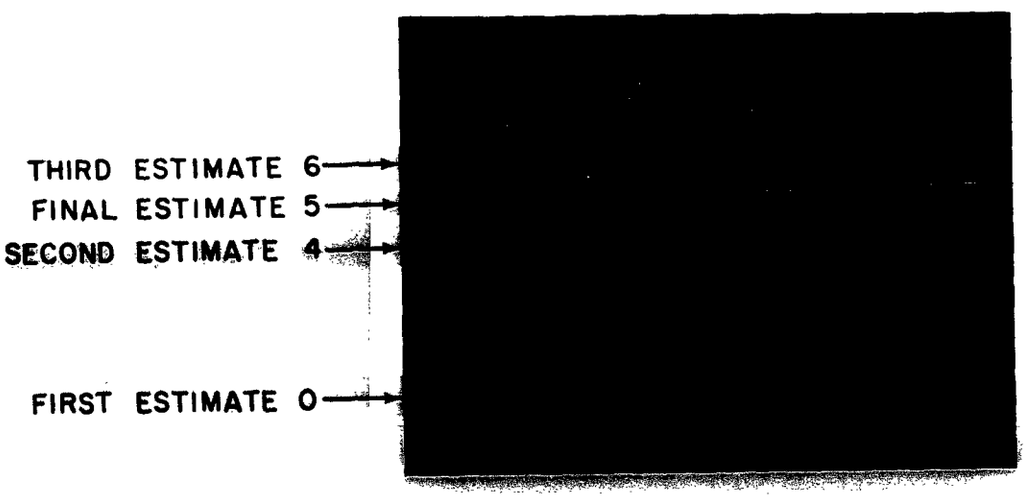


FIG. 9 COMPARATOR AND D-A CONVERTER CARD



a. 300 CPS SINE WAVE SAMPLED AT 4KC
0.5 MS/CM



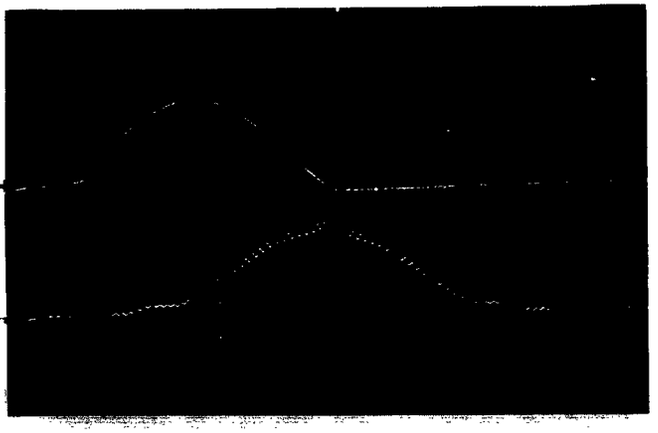
b. SAMPLING A +5 LEVEL (10 μS/CM)

FIG. 10

a.

INPUT TO FILTER

MATCHED FILTER OUTPUT
2 MS/CM



b.

FILTER INPUT HALF SINE
PULSE PLUS WHITE NOISE
0-2000 CPS 5 MS / CM

c.

MATCHED FILTER OUTPUT
5 MS/CM

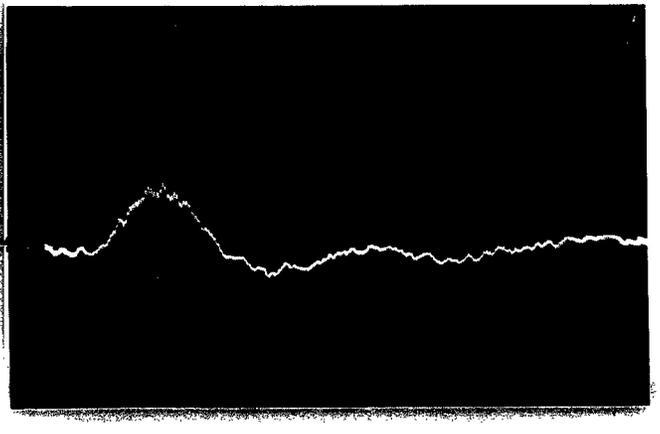


FIG. 11

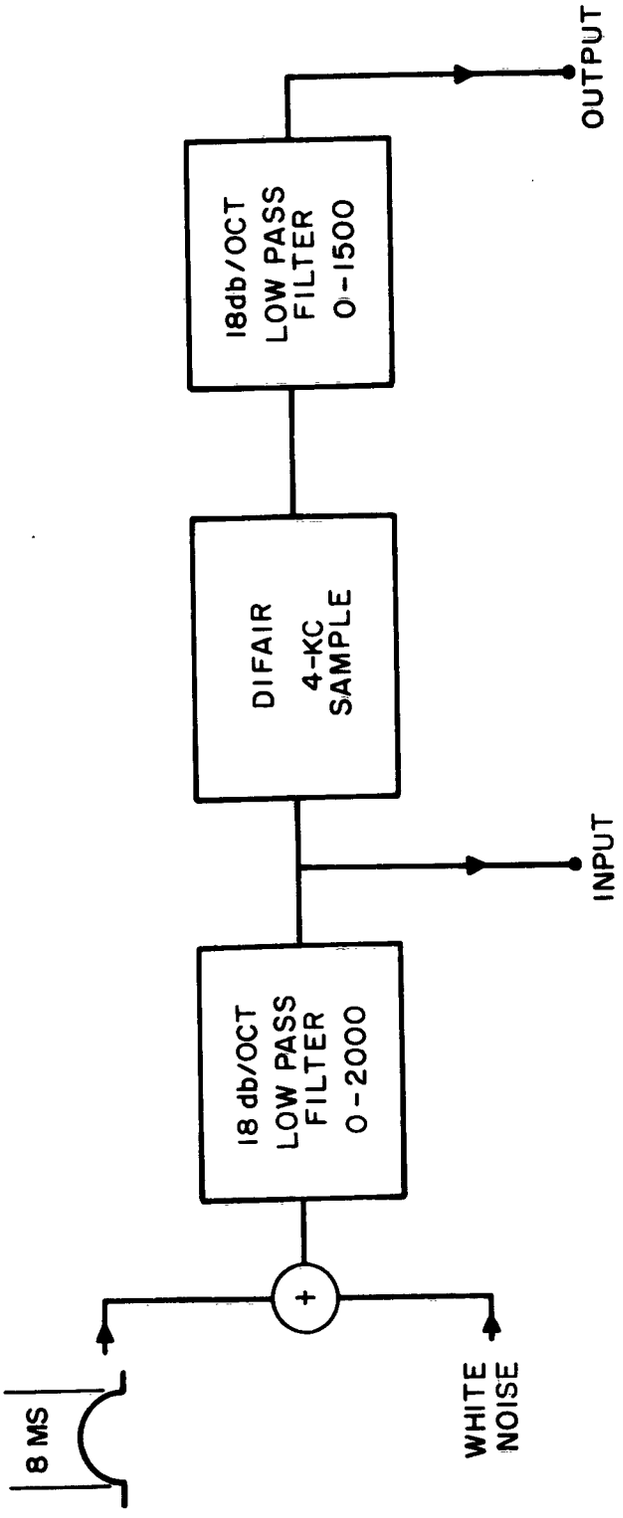


FIG. 12 MATCHED FILTER EXPERIMENTAL SETUP FOR DETECTION OF HALF-SINE PULSE

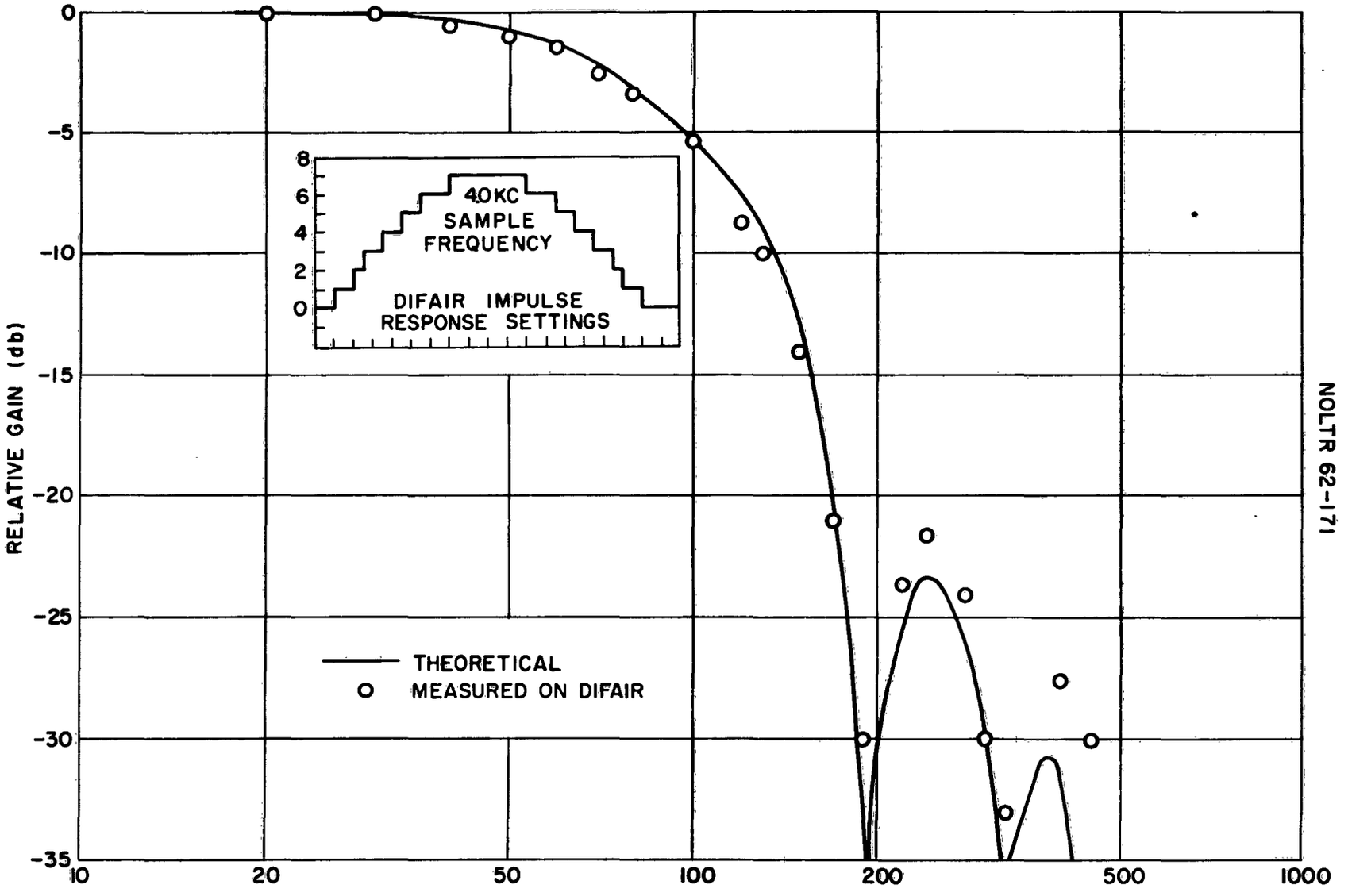


FIG. 13 SPECTRUM OF HALF SINE PULSE

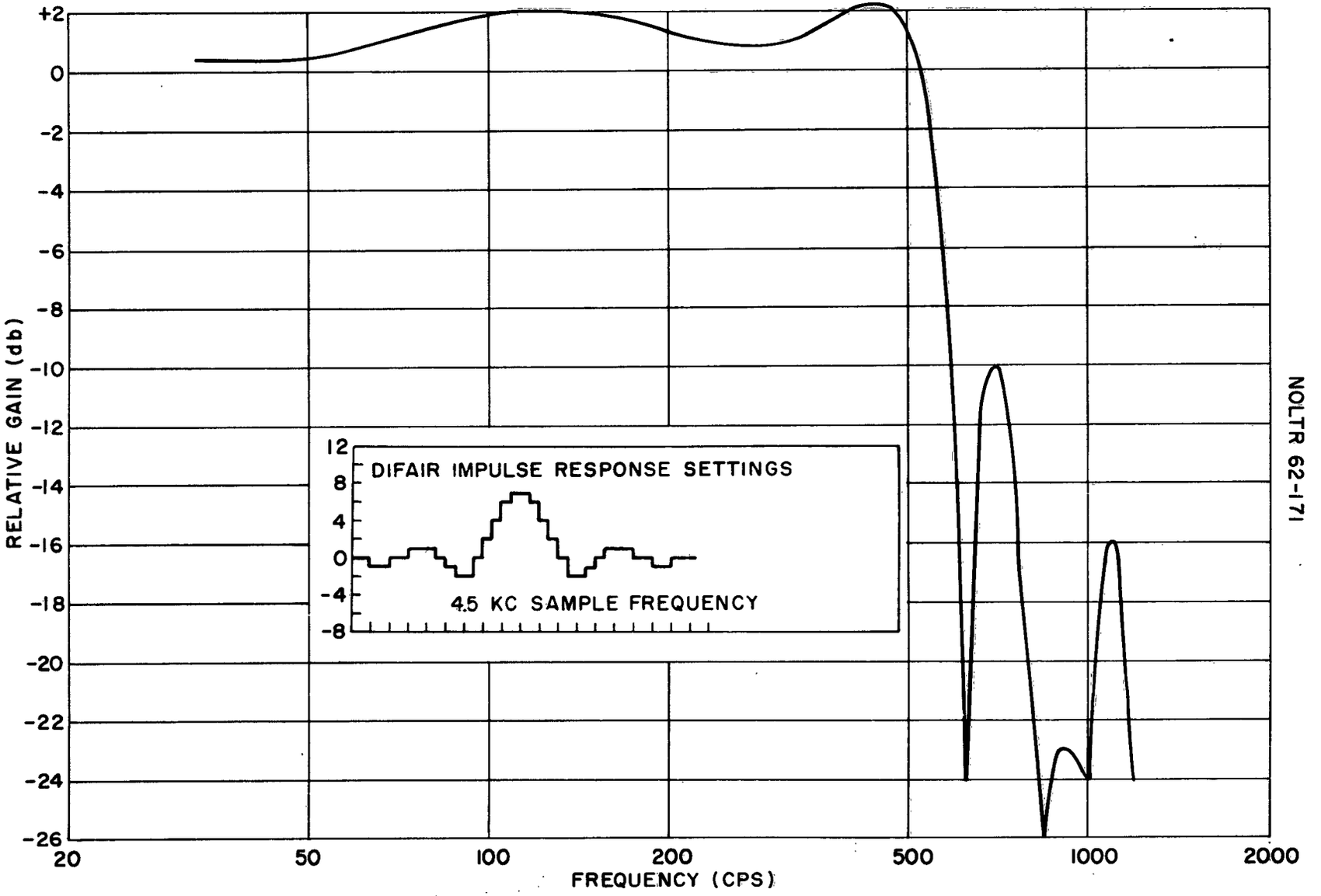


FIG. 14 SHARP CUTOFF FILTER FREQUENCY RESPONSE

TABLE I

SAMPLING FREQUENCY AND IMPULSE RESPONSE DURATION VERSUS FREQUENCY SELECTOR SWITCH SETTINGS

COARSE FREQ / FINE FREQ	A	B	C	D	E
1	1.25 CPS 25.6 SEC	10.5 CPS 3.05 SEC	83 CPS 384 MS	525 CPS 60.4 MS	4.08 KC 7.84 MS
2	2.2 CPS 17.7 SEC	15.1 CPS 2.12 SEC	120 CPS 266 MS	763 CPS 42.0 MS	5.88 KC 5.45 MS
3	2.51 CPS 12.7 SEC	20.9 CPS 1.53 SEC	166 CPS 192 MS	1.05 KC 30.3 MS	8.00 KC 4.00 MS
4	3.55 CPS 9.0 SEC	29.6 CPS 1.08 SEC	234 CPS 136 MS	1.48 KC 21.6 MS	11.1 KC 2.89 MS
5	5.30 CPS 6.0 SEC	44.0 CPS 725 MS	348 CPS 92 MS	2.19 KC 14.6 MS	15.8 KC 2.02 MS
6	7.88 CPS 4.05 SEC	65.4 CPS 490 MS	512 CPS 62.5 MS	3.18 KC 10.0 MS	22.7 KC 1.40 MS

(POTENTIOMETER ON MV-30 SET FOR MINIMUM FREQUENCY)

TABLE 2

MULTIPLIER LOGICAL CHARACTERISTICS

		INPUT 1							
		0	1	2	3	4	5	6	7
INPUT 2	0	0	0	0	0	0	0	0	0
	1	0	0	0	0	1	1	1	1
	2	0	0	1	1	1	1	2	2
	3	0	0	1	1	2	2	3	3
	4	0	1	1	2	2	3	3	4
	5	0	1	1	2	3	4	4	5
	6	0	1	2	3	3	4	5	6
	7	0	1	2	3	4	5	6	7

MULTIPLIER INPUT-OUTPUT CHARACTERISTICS

MULTIPLIER OUTPUT FUNCTIONS

INPUT 1 = BCD INPUT 2 = NPQ OUTPUT = XYZ

$$X = BN(PQ + DQ + DP + CQ + CP + CD)$$

$$Y = B\bar{C}\bar{D}N(\bar{P}+\bar{Q}) + BN\bar{P}\bar{Q}(\bar{C}+\bar{D}) + B\bar{N}P(C+Q) + \bar{B}CN(D+P) + CP(BD+NQ)$$

$$Z = \bar{C}DN\bar{P}\bar{Q} + \bar{B}C\bar{D}N\bar{P} + B\bar{C}\bar{D}\bar{P}Q + B\bar{C}\bar{N}P\bar{Q} + \bar{B}\bar{C}DN + \bar{B}C\bar{N}P + B\bar{N}\bar{P}Q + DNPQ + BCDQ + B\bar{D}NP\bar{Q} + BC\bar{D}N\bar{Q} + C\bar{N}PQ + \bar{B}CDP$$

DISTRIBUTION

	Copies
Chief, Bureau of Naval Weapons (RUSD-4) Washington 25, D. C.	
Chief, Bureau of Naval Weapons (R-14) Washington 25, D. C.	
Chief, Bureau of Naval Weapons (R-12) Washington 25, D. C.	
Chief, Bureau of Naval Weapons (RU-2) Washington 25, D. C.	
Chief, Bureau of Naval Weapons (RUDC-1) Washington 25, D. C.	
Chief, Bureau of Naval Weapons (DLI-3) Washington 25, D. C.	4
Chief, Office of Naval Research (Code 411) Washington 25, D. C.	
Chief, Office of Naval Research (Code 466) Washington 25, D. C.	
Chief of Naval Operations (Op 311) Washington 25, D. C.	
Chief of Naval Operations (Op 312) Washington 25, D. C.	
Chief of Naval Operations (Op 93R) Washington 25, D. C.	
Commander U. S. Naval Ordnance Test Station 3202 East Foothill Boulevard Pasadena, California	
Commanding Officer U. S. Naval Underwater Ordnance Station Newport, Rhode Island	
Commanding Officer and Director U. S. Navy Electronics Laboratory San Diego 52, California	

DISTRIBUTION

Copies

Commanding Officer and Director
U. S. Navy Underwater Sound Laboratory
Fort Trumbull
New London, Connecticut

Commanding Officer and Director
David Taylor Model Basin
Washington 7, D. C.

Commander
U. S. Naval Ordnance Test Station
China Lake, California

Commanding Officer and Director
Naval Research Laboratory (Code 2021)
Washington 25, D. C.

Commanding Officer and Director
Naval Research Laboratory (Code 4000)
Washington 25, D. C.

Director
Woods Hole Oceanographic Institution
Woods Hole, Massachusetts

Director
Applied Physics Laboratory
Johns Hopkins University
8621 Georgia Avenue
Silver Spring, Maryland

Director
Ordnance Research Laboratory
Pennsylvania State College
University Park, Pennsylvania

Director
Scripps Institution of Oceanography
University of California
La Jolla, California

Director
Applied Physics Laboratory
University of Washington
Seattle 5, Washington

DISTRIBUTION

	Copies
Director Hudson Laboratory Columbia University Dobbs Ferry, New York	
Director Marine Physical Laboratory San Diego, California	
National Research Council Committee on Undersea Warfare Executive Secretary 2010 Constitution Avenue, N. W. Washington 25, D. C.	
Armed Services Technical Information Agency Arlington Hall Station Arlington 12, Virginia	10

CATALOGING INFORMATION FOR LIBRARY USE

BIBLIOGRAPHIC INFORMATION

	DESCRIPTORS	CODES		DESCRIPTORS	CODES
SOURCE	NOL teshnical report	NOLTR	SECURITY CLASSIFICATION AND CODE COUNT	Unclassified - 35	UØ35
REPORT NUMBER	62-171	62Ø171	CIRCULATION LIMITATION		
REPORT DATE	27 September 1962	Ø962	CIRCULATION LIMITATION OR BIBLIOGRAPHIC		
			BIBLIOGRAPHIC (SUPPL., VOL., ETC.)		

SUBJECT ANALYSIS OF REPORT

DESCRIPTORS	CODES	DESCRIPTORS	CODES	DESCRIPTORS	CODES
Difair	DIFA	Filter (Design)	FILTD	Analog	ANAG
Matched	CMRI	Generalized	GENA	Converter	CNVR
Digital	DIGI	Frequency	FREQ	Deltic	DELT
Filters	FILT	Amplitude	AMPI	Loops	LOOP
Signals	SIGN	Spectrum	SPER	Generator	GENR
Impulse	IMPL	Waveform	WAVF	Analysis	ANAL
Response	RESP	Circuits	CIRC	Time	TIME
Computation	COMA	Electronics	ELCO	Domain	DOMA
Integral	INTE	Acoustics	ACOU	Synthesis	SYNS
Selector	SLEC	Filter (Characteristics)	FILTC	Applications	APPI
Switches	SWIT	Components	COMO	Mathematics	MATH
Computer	COMP	Multiplier	MULP		

Naval Ordnance Laboratory, White Oak, Md.
(NOL technical report 62-171)
DIFAIR, AN ADJUSTABLE DIGITAL FILTER (U), by C. Nicholas Pryor. 27 Sept. 1962. 10p. illus. diagr. Task RUSD-4C000-150. UNCLASSIFIED

Many signal processing operations, such as matched filtering, call for filters having specific characteristics. These characteristics may be specified in terms of the impulse response of the filter. The present device simulates such filters by means of high-speed digital computation of the convolution integral once the desired impulse response is set into the selector switches. The circuitry, overall characteristics and several applications of the equipment are described.

1. Filters, Matched
2. Filters, Digital
I. Title
II. Pryor, C. Nicholas
III. Project

Naval Ordnance Laboratory, White Oak, Md.
(NOL technical report 62-171)
DIFAIR, AN ADJUSTABLE DIGITAL FILTER (U), by C. Nicholas Pryor. 27 Sept. 1962. 10p. illus. diagr. Task RUSD-4C000-150. UNCLASSIFIED

Many signal processing operations, such as matched filtering, call for filters having specific characteristics. These characteristics may be specified in terms of the impulse response of the filter. The present device simulates such filters by means of high-speed digital computation of the convolution integral once the desired impulse response is set into the selector switches. The circuitry, overall characteristics and several applications of the equipment are described.

1. Filters, Matched
2. Filters, Digital
I. Title
II. Pryor, C. Nicholas
III. Project

Naval Ordnance Laboratory, White Oak, Md.
(NOL technical report 62-171)
DIFAIR, AN ADJUSTABLE DIGITAL FILTER (U), by C. Nicholas Pryor. 27 Sept. 1962. 10p. illus. diagr. Task RUSD-4C000-150. UNCLASSIFIED

Many signal processing operations, such as matched filtering, call for filters having specific characteristics. These characteristics may be specified in terms of the impulse response of the filter. The present device simulates such filters by means of high-speed digital computation of the convolution integral once the desired impulse response is set into the selector switches. The circuitry, overall characteristics and several applications of the equipment are described.

1. Filters, Matched
2. Filters, Digital
I. Title
II. Pryor, C. Nicholas
III. Project

Naval Ordnance Laboratory, White Oak, Md.
(NOL technical report 62-171)
DIFAIR, AN ADJUSTABLE DIGITAL FILTER (U), by C. Nicholas Pryor. 27 Sept. 1962. 10p. illus. diagr. Task RUSD-4C000-150. UNCLASSIFIED

Many signal processing operations, such as matched filtering, call for filters having specific characteristics. These characteristics may be specified in terms of the impulse response of the filter. The present device simulates such filters by means of high-speed digital computation of the convolution integral once the desired impulse response is set into the selector switches. The circuitry, overall characteristics and several applications of the equipment are described.

1. Filters, Matched
2. Filters, Digital
I. Title
II. Pryor, C. Nicholas
III. Project